IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method of effectively extracting a clock signal from a data stream, comprising the steps of:

generating a plurality of multiphase clock signals, wherein said plurality of multiphase clock signals operates at a first clock rate;

generating a plurality of retime states by logically combining said plurality of multiphase clock signals and a data stream, wherein said data stream operates at a second clock rate, wherein said second clock rate is an integer N times faster than said first clock rate, wherein said integer N is at least 2;

selecting one of ~~the~~ said plurality of multiphase clock signals based on a said plurality of ~~synchronization states~~ retime states identifying which of ~~the~~ said plurality of multiphase clock signals is most closely aligned with ~~the~~ said data stream; and

sampling ~~the~~ said data stream using ~~the~~ said selected one of ~~the~~ said plurality of multiphase clock signals to produce a retimed data signal.

2. (currently amended) The method of Claim 1 wherein said generating step generates said plurality of multiphase clock signals which are subharmonics of the data stream.

3. (currently amended) The method of Claim 1 wherein said selecting step includes the step of determining whether ~~the~~ said plurality of multiphase clock signals are either early or late with respect to ~~the~~ said data stream.

4. (currently amended) The method of Claim 3 wherein said determining step includes the further step of sampling ~~the~~ said plurality of multiphase clock signals using a plurality of D-type flip-flops.

5. (currently amended) The method of Claim 1 wherein ~~further comprises the steps of: each of the multiphase clock signals has at least one rising edge; and~~

~~said selecting step includes the step of using the synchronization states to define which of the rising edges of the multiphase clock signals is most closely aligned with an edge of the data stream.~~

said data stream includes at least one of a set of a first or second transition type;

wherein said plurality of multiphase clock signals includes at least one first transition type; and

said selecting comprises one of said plurality of multiphase clock signals by utilizing said plurality of retime states to determine which one of said plurality of multiphase clock signals includes at least one first transition type most closely aligned with a first or second transition type of said data stream.

6. (currently amended) The method of Claim 1 wherein said generating step generates ~~the~~ said plurality of multiphase clock signals using a multiphase voltage-controlled oscillator.

7. (currently amended) The method of Claim 6 further comprising the steps of:

creating an error signal using ~~the~~ said plurality of multiphase clock signals and ~~the~~ said data stream;

applying ~~the~~ said error signal to a charge pump; and

correcting ~~the~~ said plurality of multiphase clock signals using a control voltage output of ~~the~~ said charge pump.

8. (currently amended) The method of Claim 1 wherein said selecting step includes the step of using ~~the~~ said plurality of ~~synchronization states~~ retime states to define a plurality of retime state signals.

9. (currently amended) The method of Claim 8 wherein said sampling step further comprises the steps of:

inverting ~~the~~ said plurality of multiphase clock signals to produce a plurality of inverted phase signals;

combining respective pairs of ~~the~~ said plurality of retime state signals and ~~the~~ said plurality of inverted phase signals ~~using~~ utilizing a plurality of respective AND gates;

combining the outputs of ~~the~~ said plurality of AND gates ~~using~~ utilizing an OR gate; and

latching the output of ~~the~~ said OR gate using ~~the~~ said data stream to produce ~~the~~ said retimed data signal.

10. (currently amended) A circuit for effectively extracting a clock signal from a data stream, comprising:

means for generating a plurality of multiphase clock signals, wherein said plurality of multiphase clock signals operates at a first clock rate;

means for generating a plurality of retime states by logically combining said plurality of multiphase clock signals and a data stream, wherein said data stream operates at a second clock rate, wherein said second clock rate is an integer N times faster than said first clock rate, wherein said integer N is at least 2;

means for selecting one of ~~the~~ said plurality of multiphase clock signals based on ~~a~~ said plurality of ~~synchronization states~~ retime states identifying which of ~~the~~ said multiphase clock signals is most closely aligned with ~~the~~ said data stream; and

means for sampling ~~the~~ said data stream using ~~the~~ said selected one of ~~the~~ said plurality of multiphase signals to produce a retimed data signal.

11. (currently amended) The circuit of Claim 10 wherein said generating means generates said plurality of multiphase clock signals which are subharmonics of ~~the~~ said data stream.

12. (currently amended) The circuit of Claim 10 wherein said selecting means includes means for determining whether ~~the~~ said plurality of multiphase clock signals are either early or late with respect to ~~the~~ said data stream.

13. (currently amended) The circuit of Claim 12 wherein said determining means samples ~~the~~ said plurality of multiphase clock signals using a plurality of D-type flip-flops.

14. (currently amended) The circuit of Claim 10 wherein:

~~each of the multiphase clock signals has at least one rising edge; and~~

~~said selecting means uses the synchronization states to define which of the rising edges of the multiphase clock signals is most closely aligned with an edge of the data stream.~~

said data stream includes at least one of a set of a first or second transition type;

said plurality of multiphase clock signals includes at least on first transition type; and

said means for selecting comprises selecting one of said plurality of multiphase clock signals by utilizing said plurality of retime states to determine which one of said plurality of multiphase clock signals includes at least one first transition type most closely aligned with a first or second transition type of said data stream.

15. (original) The circuit of Claim 10 wherein said generating means includes a multiphase voltage-controlled oscillator.

16. (currently amended) The circuit of Claim 15 further comprising:

means for creating an error signal ~~using~~ utilizing ~~the~~ said plurality of multiphase clock signals and ~~the~~ said data stream; and

a charge pump receiving ~~the~~ said error signal as an input, and providing a control voltage output to said voltage-controlled oscillator.

17. The circuit of Claim 10 wherein said selecting means ~~uses~~ utilizes ~~the~~ said ~~synchronization states~~ retime states to define a plurality of retime state signals.

18. (currently amended) The circuit of Claim 17 wherein said sampling means further comprises:

means for inverting ~~inverts~~ ~~the~~ said plurality of multiphase clock signals to produce a plurality of inverted phase signals;

means for ~~combines~~ combining respective pairs of ~~the~~ said plurality of retime state signals and ~~the~~ said plurality of inverted phase signals using a plurality of respective AND gates;

means for further ~~combines~~ combining outputs of said plurality of respective AND gates using an OR gate; and

means for ~~latches~~ latching an output of said OR gate using the data stream to produce ~~the~~ said retimed data signal.

19. (new) The method of Claim 1, wherein said selecting step further comprises the step of:

selecting another one of said plurality of multiphase clock signals at each first or second transition type of said data stream.

20. (new) The circuit of Claim 10, wherein said means for selecting further comprises:

means for selecting another one of said plurality of multiphase clock signals at each first or second transition type of said data stream.

21. (new) The method of Claim 1, wherein:

said method further comprises determining if said data stream transitions during one of said plurality of retime states; and

wherein said sampling step comprises timing said retimed data signal with one of said plurality of multiphase clock signals corresponding to one of said plurality of retime states, in response to determining that said data stream transitions during one of said plurality of retime states.

22. (new) The circuit of Claim 10, wherein:

said circuit further comprises a means for determining if said data stream transitions during one of said plurality of retime states; and

wherein said means for sampling comprises a means for timing said retimed data signal with one of said plurality of multiphase clock signals corresponding to one of said plurality of retime states, in response to determining that said data stream transitions during one of said plurality of retime states.